WHAT IS CLAIMED IS:

1. A circuit, comprising:

a clock transmitter in communication with a clock bus, the clock transmitter to transmit a clock signal on the clock bus;

a clock receiver in communication with the clock bus, the clock receiver to receive a clock signal on the clock bus; and

a driver in communication with the clock bus, the driver to drive a voltage of the clock bus to a first voltage level when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

2. The circuit of claim 1, wherein the first voltage level is a voltage level corresponding to a logical one.

3. The circuit of claim 1, wherein the driver includes a resistance.

4. The circuit of claim 3, wherein the driver includes a first resistance between the clock bus and a voltage V_{DD}, and wherein the driver further includes a second resistance between the clock bus and ground.

5. The circuit of claim 1, wherein the driver includes a transistor.

6. The circuit of claim 1, further including enabling circuitry in communication with the driver, the enabling circuitry to enable the driver when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

7. The circuit of claim 6, the enabling circuitry further to disable the driver when the clock transmitter is not transmitting a clock signal on the clock bus and the clock receiver is not receiving a clock signal on the clock bus.

8. The circuit of claim 6, further including receive processing circuitry in communication with the enabling circuitry, the receive processing circuitry including a receive processing clock, the receive processing clock to turn off in response to a signal from the enabling circuitry.

9. The circuit of claim 6, wherein the enabling circuitry includes a flip flop.

10. The circuit of claim9, wherein the enabling circuitry enables the driver when the flip flop is in a first state, and wherein the enabling circuitry disables the driver when the flip flop is in a second state.

11. The circuit of claim 1, wherein the driver is included in a packet processor.

12. The circuit of claim 1, wherein the driver is included in a packet processor configured to transmit data and to receive data according to a double data rate protocol.

13. The circuit of claim 12, further including a memory.

14. The circuit of claim 13, wherein the memory is configured to transmit data and to receive data according to the double data rate protocol.

15. The circuit of claim 13, wherein the memory includes:

another clock transmitter in communication with the clock bus, the another clock transmitter to transmit a clock signal on the clock bus;

another clock receiver in communication with the clock bus, the another clock receiver to receive a clock signal on the clock bus; and

another driver in communication with the clock bus, the another driver to drive the voltage of the clock bus to the first voltage level when the another clock transmitter is not transmitting a clock signal on the clock bus and the another clock receiver is not receiving a clock signal on the clock bus.

16. A data transfer method, comprising:

(a) determining that no device is transmitting a clock signal on a clock bus;

(b) after (a), driving a clock bus to a first voltage;

(c) determining that the voltage of the clock bus is equal to the first voltage; and

(d) after (c), driving the clock bus to a second voltage different than the first voltage.

17. The method of claim 16, wherein the first voltage corresponds to a logical one and the second voltage corresponds to a logical zero.

18. The method of claim 16, further comprising:

(e) after (d), driving a clock signal on the clock bus, wherein driving the clock signal comprises driving the clock bus to the first voltage and the second voltage alternately.

19. The method of claim 18, further comprising:

(f) driving a data signal on a data bus, the data signal synchronized with the clock signal.

20. The method of claim 18, wherein driving the data signal on the data bus comprises driving a first data bit synchronously with a rising edge of the clock signal.

21. The method of claim 20, wherein driving the data signal on a data bus comprises driving a second data bit synchronously with a falling edge of the clock signal.

22. The method of claim 16, further comprising disabling the driver.

23. A circuit, comprising:

a clock signal transmission means in communication with a clock bus, the clock signal transmission means for transmitting a clock signal on the clock bus;

a clock signal receiving means in communication with the

clock bus, the clock signal receiving means for receiving a clock signal on the clock bus; and

a voltage driving means in communication with the clock bus, the voltage driving means for driving a voltage of the clock bus to a first voltage level when the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

24. The circuit of claim 23, wherein the first voltage level is a voltage level corresponding to a logical one.

25. The circuit of claim 23, wherein the voltage driving means includes a resistance means.

26. The circuit of claim 25, wherein the voltage driving means includes a first resistance means between the clock bus and a voltage V_{DD}, and wherein the voltage driving means further includes a second resistance means between the clock bus and ground.

27. The circuit of claim 23, wherein the voltage driving means includes a transistor.

28. The circuit of claim 23, further including enabling means in communication with the voltage driving means, the enabling means for enabling the voltage driving means when the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

29. The circuit of claim 28, the enabling means further for disabling the voltage driving means when the clock signal transmission means is not transmitting a clock signal on the clock bus and the clock signal receiving means is not receiving a clock signal on the clock bus.

30. The circuit of claim 28, further including receive processing means in communication with the enabling means, the receive processing means including a receive processing clock means, the receive processing clock means to turn off in response to a signal from the enabling means.

31. The circuit of claim 28, wherein the enabling means includes a flip flop.

32. The circuit of claim 31, wherein the enabling means enables the driving means when the flip flop is in a first

state, and wherein the enabling means disables the driver when the flip flop is in a second state.

33. The circuit of claim 23, wherein the voltage driving means is included in a packet processing means.

34. The circuit of claim 33, wherein the packet processing means is for transmitting data and for receiving data according to a double data rate protocol.

35. The circuit of claim 34, further including a memory means.

36. The circuit of claim 35, wherein the memory means is for transmitting data and for receiving data according to the double data rate protocol.

37. The circuit of claim 35, wherein the memory means includes:

another clock signal transmission means in communication with a clock bus, the another clock signal transmission means for transmitting a clock signal on the clock bus;

another clock signal receiving means in communication with the clock bus, the another clock signal receiving means

for receiving a clock signal on the clock bus; and

another voltage driving means in communication with the clock bus, the another voltage driving means for driving a voltage of the clock bus to a first voltage level when the another clock signal transmission means is not transmitting a clock signal on the clock bus and the another clock signal receiving means is not receiving a clock signal on the clock bus.